

(21) Application No 9424190.8

(22) Date of Filing 30.11.1994

(30) Priority Data

(31) 9324534

(32) 30.11.1993

(33) GB

(71) Applicant(s)

GEC-Marconi Limited

(Incorporated in the United Kingdom)

The Grove, Warren Lane, STANMORE, Middlesex,  
HA7 4LY, United Kingdom

(72) Inventor(s)

Ian James Forster

(74) Agent and/or Address for Service

Jonathan Rodwell

GEC Patent Department, Waterhouse Lane,  
CHELMSFORD, Essex, CM1 2QX, United Kingdom

(51) INT CL<sup>6</sup>

G01S 13/82, H03C 1/36

(52) UK CL (Edition N )

H4L LADCS

H3R RADR RADX

(56) Documents Cited

EP 0486367 A1

(58) Field of Search

UK CL (Edition N ) H3R RADB RADC RADD RADR

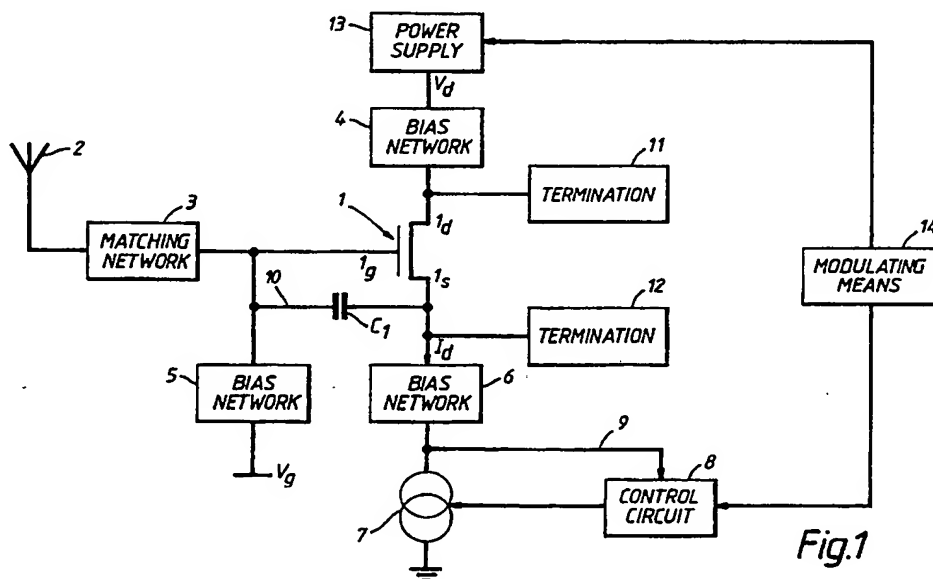
RADX, H4D DRSA DRSB, H4L LADCS LADTA

INT CL<sup>6</sup> G01S 13/82, H03C 1/36

Online databases: WPI

(54) Tag circuit arrangement

(57) A circuit arrangement, particularly for use with a transponder, comprises a transistor (1) configured to detect an amplitude modulated signal upon operation within the non-linear relatively low gain region (A) of the transistor's current voltage characteristic. The transistor is also configured by means of a feedback arrangement (10, C<sub>1</sub>) upon operation within a linear relatively higher current and gain region (B) of the characteristic to reflect the signal with an increased amplitude, the transistor acting as a negative resistance. The change in operating point is effected by switching the biasing network  $\alpha$  (6, 7) values. Operation of the switch (52) while in the reflection mode is also used to modulate the reflected signal. Modulation (14) of the power supply to the transistor with a periodic waveform produces a single side band reflected signal.



1/4

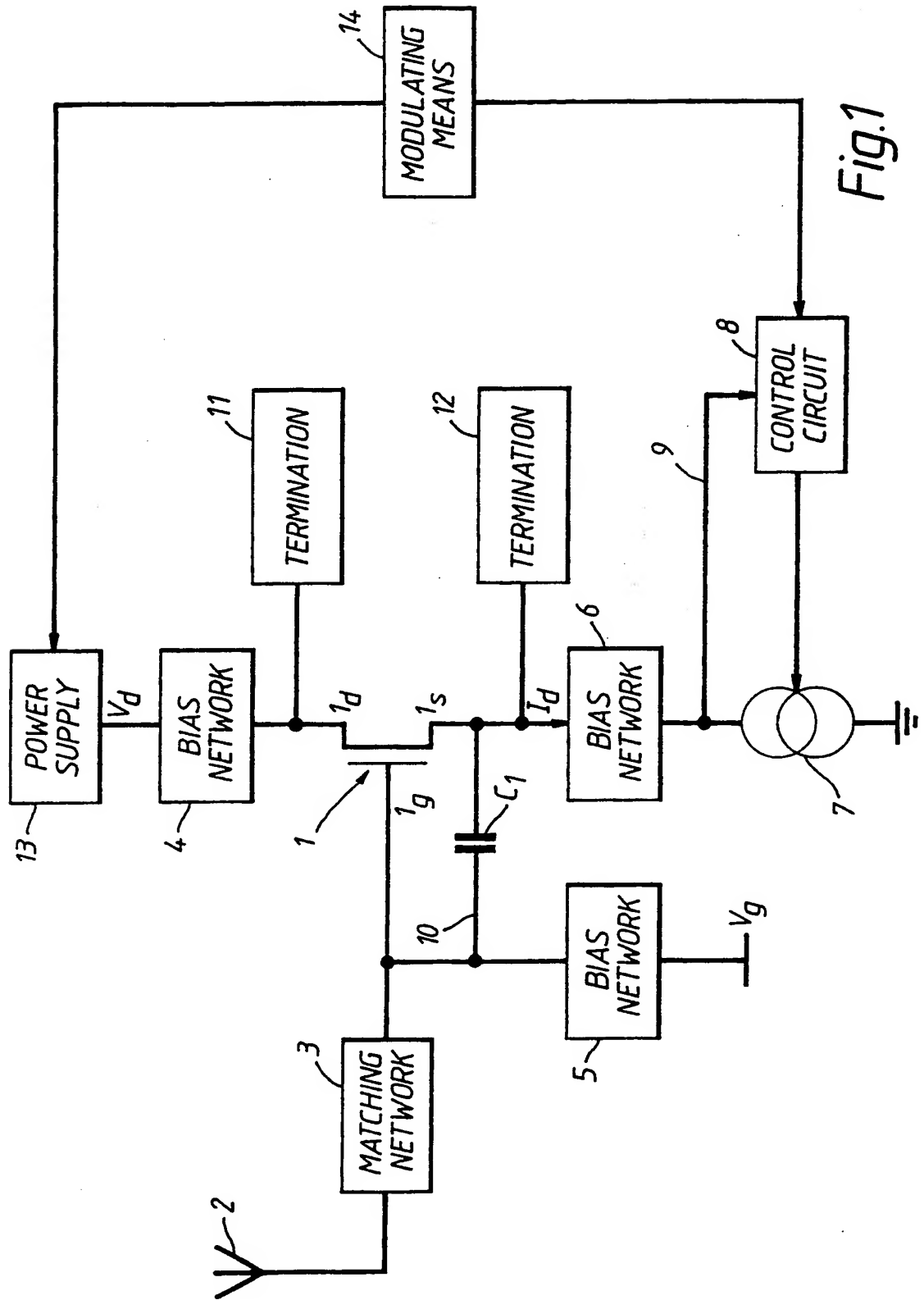


Fig. 1

2/4

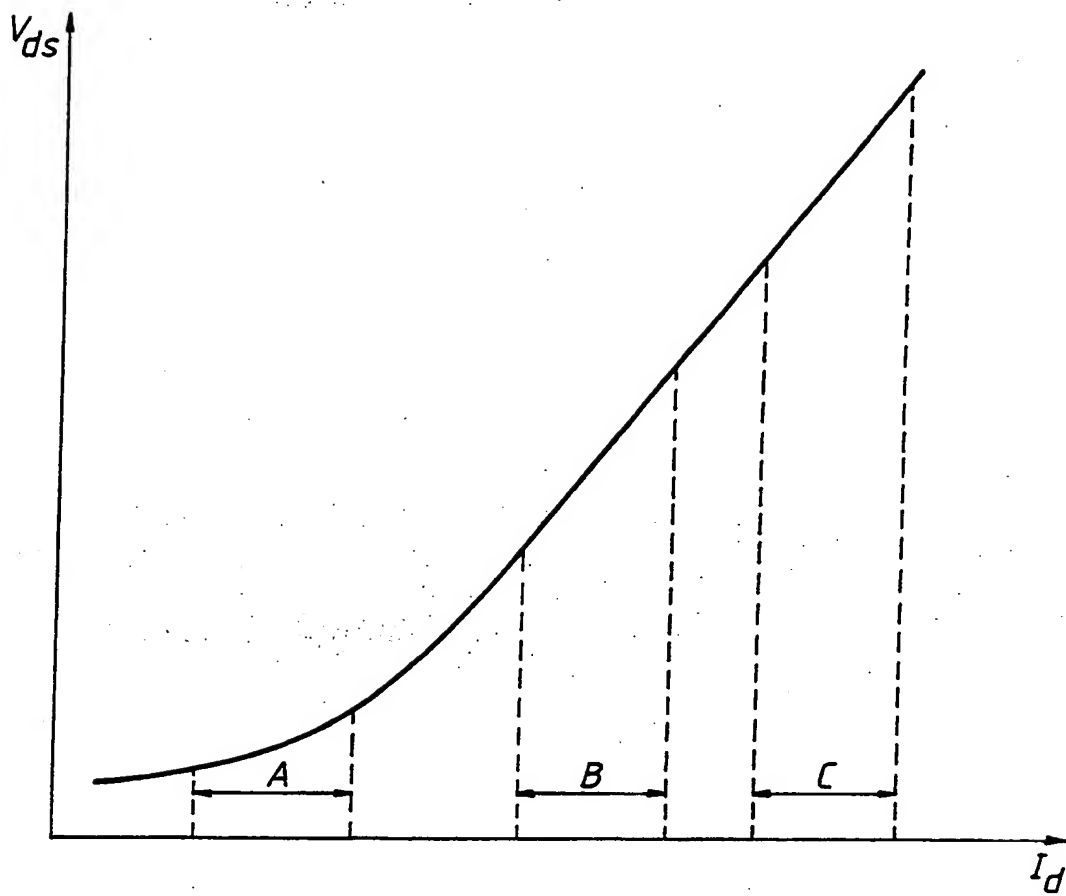


Fig.2

3/4

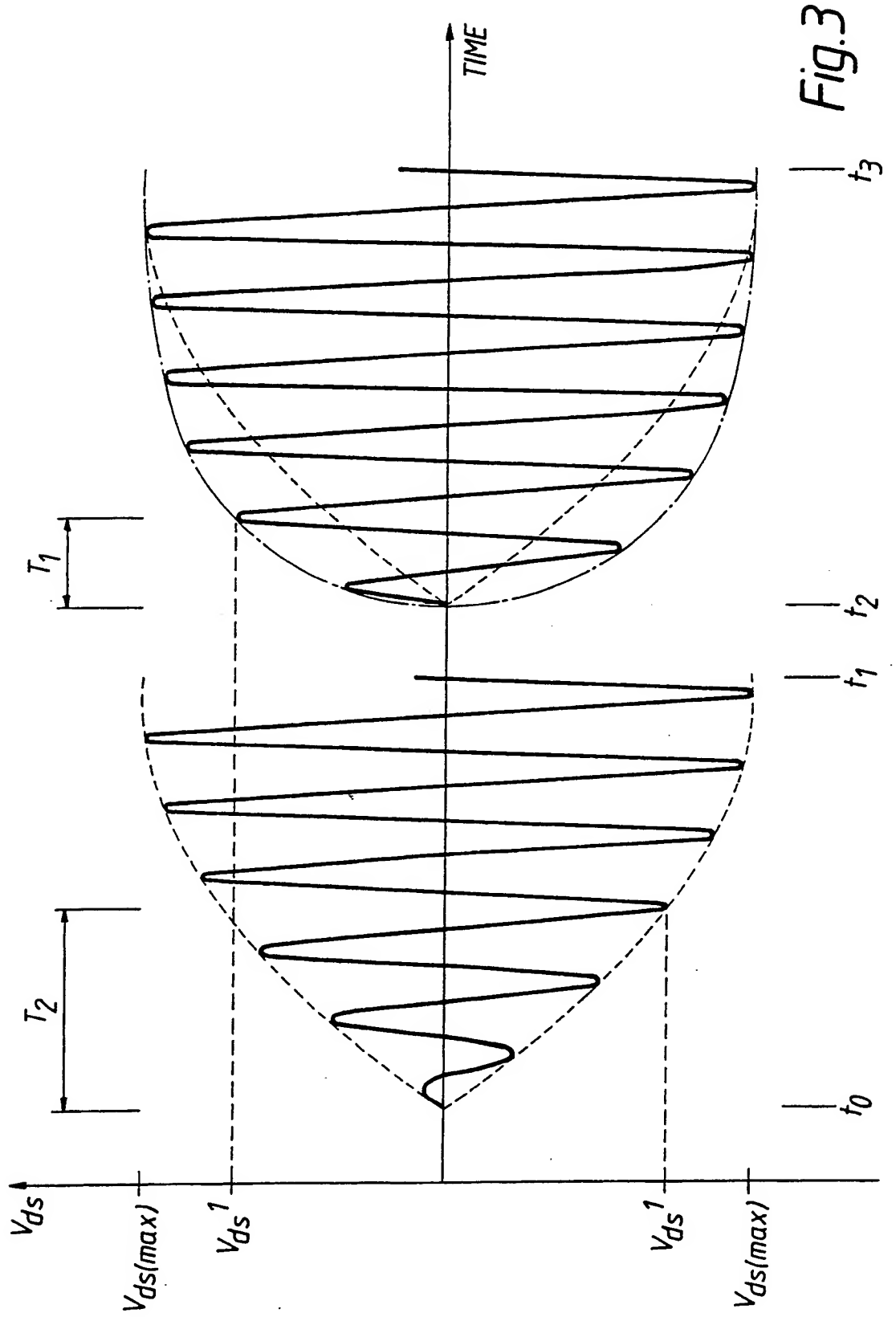


Fig.3

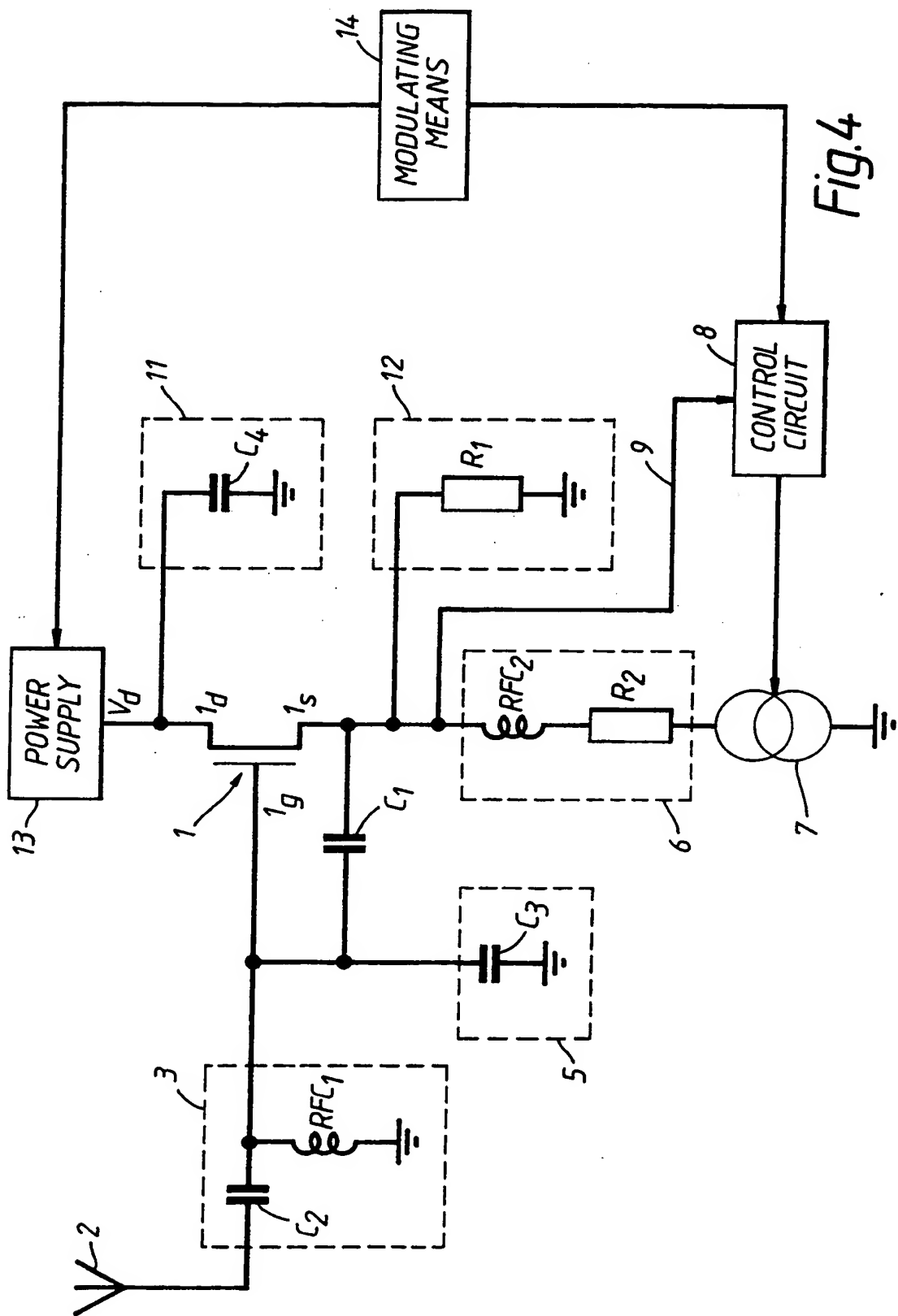


Fig. 4

CIRCUIT ARRANGEMENT

This invention relates to a circuit arrangement in particular, although not exclusively, for use with a pseudo passive transponder (PPT).

Conventionally PPT's use a diode detector arrangement to detect an incoming signal  
5 from an interrogating source. The diode can be operated as a modulated reflector by modulating the incoming signal with information and reflecting it back to the interrogating source. The reflected signal is however of reduced amplitude with respect to the incoming signal which limits the useful range of the transponder. In addition the reflected signal has a double sideband which increases the complexity of the circuitry  
10 required at the interrogating source and reduces the spectral efficiency of the system. A need exists therefore for a circuit arrangement for use in a PPT which can be made available at relatively low cost, which can increase the available operating range, and preferably emit energy with only a single sideband.

15 This invention provides a circuit arrangement comprising a transistor configured to detect an amplitude modulated signal upon operation within the non-linear relatively low gain region of the transistors current/voltage characteristic, the transistor also being configured by means of a feedback arrangement upon operation within a linear relatively higher current and gain region of the characteristic to reflect the signal with an increased  
20 amplitude.

Surprisingly, the applicants have found that a single transistor can be used both as a so

called "cold cathode" detector and a reflective amplifier merely by changing the operating conditions of the transistor. As compared to the known diode arrangement, there need not be a significant increase in power consumption.

- 5 In a preferred embodiment, the transistor is a field effect transistor (FET) which is switchable between the detect and reflect modes by increasing the drain/source current. With such a device, when operated at microwave frequencies, the feedback can be provided via the intrinsic capacitance between the gate and source of the FET.
- 10 According to another aspect of the present invention there is provided a modulated reflector circuit arrangement comprising a transistor configured by means of a feedback arrangement upon operation within a linear region of the transistor's current/voltage characteristic to reflect an incoming amplitude modulated signal with an increased amplitude and modulating means operable to modulate power to the transistor with a
- 15 periodic waveform in which the reciprocal of the period of the periodic waveform is the required sideband frequency of the reflected signal and the waveform is selected such that the arrangement reflects a substantially single sideband signal.

In order that the invention may be well understood, embodiments thereof will now be  
20 described by way of example with reference to the accompanying drawings, in which;

Figure 1 is a schematic circuit diagram of a circuit arrangement;

Figure 2 shows a typical voltage/current characteristic of a FET;

Figure 3 shows the detected signal in another mode of operation; and

Figure 4 is a circuit diagram of a circuit arrangement for use at UHF frequencies.

5 As shown in Figure 1 a circuit arrangement comprises a field effect transistor 1, which can for example be either a silicone JFET or a GaAs device, depending on the required operating frequency. An antenna 2 supplies a signal via a matching network 3 to the gate  $1_g$  of the transistor. The drain  $1_d$  is connected via a bias network 4 to a power supply 13 producing a rail voltage  $V_d$ . The bias conditions on the gate side are set by  
10 means of an appropriate bias network 5 connected to a voltage rail  $V_g$ . The source  $1_s$  is connected via a bias network 6 to a variable current source 7 which is itself connected to a control circuit 8. The bias networks 4, 5, 6 provide isolation between the relatively low voltage, low frequency signals on the control side, and the typically much higher frequencies with which a transponder is designed to operate.

15

An output 9 is taken from the source side of the transistor from beyond the bias network 6. Termination circuitry 11, 12 is provided on the drain and source sides. The exact nature of the components will vary depending upon the frequency of operation, but essentially the networks 11, 12 determine the frequency and phase characteristics of the  
20 circuit.

A feedback arrangement is provided by a line 10 and capacitor  $C_1$ . At microwave frequencies it is possible by appropriate selection of the termination circuitry 11, 12 to exploit the intrinsic capacitance between the gate  $1_g$  and source  $1_s$  to provide the



feedback capacitance  $C_1$ .

The variable current source 7 can be used under control of control circuit 8 to alter the drain source bias current and thereby cause the circuit to operate in one of three modes as will now be described with reference to Figure 2. Figure 2 shows the typical variation in drain source voltage  $V_{ds}$  with drain current  $I_d$ , the so-called transconductance curve of a FET. With the transistor operating within the non linear relatively low gain region A it can, as is well known, thereby act as a detector by amplifying higher amplitude signals relatively more than lower amplitude signals. Increasing the drain current further the transistor operates in the linear relatively higher current and gain region B due to the feedback provided on line 10 and by capacitor  $C_1$ . The transistor then acts as a negative resistance or amplifier reflecting any incoming signals with an increased amplitude. Information can be transmitted to an interrogation source by modulating the drain source current using the variable current source 7 and control circuit 8. Unlike the prior art diode arrangements, the amplitudes of the information carrying sidebands of the reflected signal when operated as a modulated reflector can be greater than the incoming signal.

As with the prior art diode arrangement the present invention when operated as a modulated reflector produces a double sideband signal. Unlike the prior art arrangement a single sideband signal can however be produced by modulating the power to the transistor 1 with a special form of periodic waveform. Referring to Figure 1, modulating means 14 controls the power supply 13 and control circuit 8. The modulating means is configured to modulate either the drain source current and/or the rail voltage  $V_d$  with a

complex periodic waveform, for example a distorted sine wave. The periodic waveform is selected such that the reciprocal of the period of the waveform is equal to the frequency of required sideband. It has been found that modulating the current and/or voltage in this way when in its reflective mode produces a single sideband emission.

- 5 This is because the sideband energy is generated from two forms of modulation, phase and amplitude. The generated sideband pairs from the two forms of modulation have an opposite phase relationship and therefore when the amplitude of the sidebands is balanced the sidebands on one side cancel whilst the others combine resulting in a single sideband. Modulating the power to the transistor has the effect of modulating the phase
- 10 and amplitude of the reflection coefficient of the transistor. The concept of modulating the power to the transistor to produce a single sideband emission is considered inventive in itself and accordingly this concept is not restricted to a circuit arrangement which has to be operable both as a detector and as a modulated reflector.
- 15 The circuit arrangement shown in Figure 1 can also be operated as a super regenerative receiver further increasing the drain current  $I_d$  to region C. In this way the transistor becomes unstable and will oscillate. Figure 3 shows the drain source voltage  $V_{ds}$  varying with time as the variable current source 7 is switched on at times  $t_0$ ,  $t_2$  and off at  $t_1$ ,  $t_3$  by the control circuit 8. The amplitude of the oscillations increases up to a maximum
- 20 level  $V_{ds(max)}$ . The circuit can be used as a sensitive detector due to the fact that an incoming signal to the gate  $1_g$  as long as it is at the frequency of oscillation, will lead to a decrease in the rise time  $T_1$ , as compared to the rise time  $T_2$  to reach a given level of oscillation amplitude  $V_{ds}^1$  when no such signal is detected. By switching or modulating the variable current source 7 information can be transmitted back to the interrogating

source.

Figure 4 shows a circuit arrangement typically for use at UHF frequencies. The circuit is generally similar to that shown schematically in Figure 1 and the same parts are identified with the same reference numerals. The matching network 3 is provided by a capacitor  $C_2$  and a choke  $RFC_1$ . The bias network 5 is provided by a capacitor  $C_3$ . Termination networks 11, 12 are constituted by a capacitor  $C_4$  and resistor  $R_1$ . The bias network 6 on the output side is provided by a further choke  $RFC_2$  and resistor  $R_2$  connected in series.

CLAIMS

1. A circuit arrangement comprising a transistor configured to detect an amplitude modulated signal upon operation within the non-linear relatively low gain region of the transistors current/voltage characteristic, the transistor also being configured by means of a feedback arrangement upon operation within a linear relatively higher current and gain region of the characteristic to reflect the signal with an increased amplitude.
2. A circuit arrangement according to claim 1 further including modulating means operable in the higher gain region to modulate power to the transistor with a periodic waveform in which the reciprocal of the period of the periodic waveform is the required sideband frequency of the reflected signal and the waveform is selected such that the arrangement reflects a substantially single sideband signal.
3. A circuit arrangement according to claim 1 in which the transistor is a field effect transistor (FET).
4. A circuit arrangement according to claim 3 which is switchable between the detect and reflect modes by increasing the drain/source current.
5. A circuit arrangement according to claim 3 operable at microwave frequencies and in which the feedback is provided via the capacitance between the gate and source of the FET.

6. A circuit arrangement according to any preceding claim including an antenna which provides the amplitude modulated signal to the transistor.
7. A circuit arrangement according to claim 6 including means for switching into and out of the reflective mode so as to modulate the reflected signal.
8. A circuit arrangement according to any preceding claim including means for periodically further increasing the current so as to cause the transistor to oscillate.
9. A circuit arrangement according to claim 8 as dependent on claim 6 including further means for detecting an incoming signal having a frequency substantially identical to the oscillatory frequency upon a decrease in the time taken to reach the oscillating condition.
10. A circuit arrangement substantially as described with reference to the drawings.
11. A transponder including a circuit arrangement according to any preceding claim.
12. A modulated reflector circuit arrangement comprising a transistor configured by means of a feedback arrangement upon operation within a linear region of the transistor's current/voltage characteristic to reflect an incoming amplitude modulated signal with an increased amplitude and modulating means operable to modulate power to the transistor with a periodic waveform in which the reciprocal of the period of the periodic waveform is the required sideband frequency of the reflected signal and the waveform is selected

such that the arrangement reflects a substantially single sideband signal.

**Relevant Technical Fields**

(i) UK Cl (Ed.N) H4L (LADCS, LADTA); H4D (DRSA, DRSB) H3R (RADB, RADC, RADD, RADR, RADX)

(ii) Int Cl (Ed.6) G015 13/82; H03C 1/36

Search Examiner  
MR N HALLDate of completion of Search  
19 JANUARY 1995**Databases** (see below)

(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ON-LINE: WPI

Documents considered relevant following a search in respect of Claims :-  
1-11**Categories of documents**

- X: Document indicating lack of novelty or of inventive step. P: Document published on or after the declared priority date but before the filing date of the present application.
- Y: Document indicating lack of inventive step if combined with one or more other documents of the same category. E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.
- A: Document indicating technological background and/or state of the art. &: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
X,A	EP 0486367 A1 (THOMSON) & US 5305469 (CAMIADE) 19/4/94 whole document	1 at least

**Databases:** The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

**THIS PAGE BLANK (USPTO)**